REMARKS

Claims 1 to 27 were pending in the application at the time of examination. The Examiner objected to Claim 26. The Examiner rejected Claims 1 to 27 under 35 U.S.C. 103(a) as obvious over the Hobbs et al reference (2002/01991178 A1).

Applicants have amended Claims 1, 26 and 27. Claims 1 to 27 remain in the application.

OBJECTION TO Claim 26

The Examiner objected to Claim 26.

Applicants have amended Claim 26. In light of the amendment to Claim 26, Applicants' respectfully request the Examiner withdraw the objection to Claim 26.

REJECTION OF CLAIMS 1 TO 27

The Examiner rejected Claims 1 to 27 under 35 U.S.C. 103(a) as obvious over the Hobbs et al reference (2002/01991178 A1).

Applicants first submit that the Examiner is using 20/20 hindsight to equate a compiler method to avoid the specific problem of cache thrashing, i.e., prefetching data and then removing the data prior to use and then finding it is needed, with a **dynamic** cache prefetch insertion method to make an improper 103(a) rejection. To make a prima facie obviousness rejection, the MPEP directs:

> **BASIC CONSIDERATIONS WHICH APPLY TO OBVIOUSNESS REJECTIONS**
> When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to:

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(A) **The claimed invention must be considered as a whole;**
(B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
(C) **The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention;** and
(D) Reasonable expectation of success is the standard with which obviousness is determined.

MPEP § 2141, 8th Ed., Rev. 2, p. 2100-120 (May 2004). It is noted that this directive stated "the following tenets . . . **must be adhered to**." Accordingly, failure to adhere to any one of these tenets means that a prima facie obviousness rejection has not been made.

The final rejection failed to adhere to multiple of these tenets. As demonstrated more completely below, the claimed invention has not been considered as a whole; the references have not been considered as a whole; and the references do not suggest the desirability of making the combination. Pieces of the references have been extracted and selectively interpreted in view of Applicant's claims. Finally, there was no explanation of how the primary reference would work for its intended purpose following the modification.

However, even if the Examiner were not bound by the patent law and was allowed 20/20 hindsight, the Hobbs reference still fails to disclose a **dynamic** optimization as recited in Applicants' Claims.

Applicants define the term dynamic in Applicants' Specification at page 2, lines 26 to 28 as follows, with emphasis added:

> It may be desirable to **dynamically** optimize program performance. **As described herein, dynamic generally refers to actions that take place at the**

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> **moment they are needed, e.g., during runtime, rather than in advance, e.g., during compile time**.

Throughout Applicants' Specification, Applicants have repeatedly pointed out that their invention is directed a method of **dynamic** data cache prefetch insertion. For example see: Applicants' Title of the Invention; Applicants' Specification at page 2, lines 5 to 15; Applicants' Specification at page 2, lines 5 to 15; Applicants' Specification at page 3, lines 7 to 19; Applicants' Specification at page 4, line 5 and, Applicants' Specification at page 7, lines 11 to 25. This aspect of Applicants' invention is also specifically recited in Applicants' independent Claims 13 and 25, **as filed**, and implicitly recited in Applicants' Claims 1, 26 and 27, as filed.

For instance, Applicants' independent Claim 13, **as filed**, reads as follows, with emphasis added:

> A method of optimizing a program comprising a plurality of execution paths, the method comprising:
> collecting information describing a plurality of occurrences of a plurality of cache miss events **during a runtime mode of the program**;
> identifying a performance degrading execution path in the program;
> modifying the performance degrading execution path to define an optimized execution path, the optimized execution path comprising at least one prefetch instruction;
> storing the optimized execution path; and
> redirecting the performance degrading execution path in the program to include the optimized execution path.

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Applicants' independent Claim 25, **as filed**, reads as follows, with emphasis added:

> A method of optimizing a program, the method comprising:
> receiving information describing a dependency graph for an instruction causing frequent cache misses, the instruction being included in the program;
> determining whether a cyclic dependency pattern exists in the graph;
> if the cyclic dependency pattern exists then, computing stride information derived from the cyclic dependency pattern;
> inserting an at least one prefetch instruction derived from the stride information, the at least one prefetch instruction being inserted into the program prior to the instruction causing the frequent cache misses;
> reusing the at least one prefetch instruction in the program for reducing subsequent cache misses; and
> **performing said receiving, said determining, said computing, said inserting and said reusing during runtime of the program.**

In contrast to Applicants' invention as recited in the above Claims 13 and 25, **as filed,** the Hobbs et al. reference discloses, teaches and suggests "A method for **compiling** a program to reduce the possibility of cache thrashing..." (See Hobbs' Abstract, paragraph [0019], and the Hobbs Figures, as an example).

As noted above, the dynamic nature of Applicants' invention was also implicitly recited in Applicants' Claims 1, 26 and 27. However, in order to expedite prosecution of this case, Applicants have amended Claims 1, 26 and 27 to explicitly recite this feature. Applicants' independent Claim 1, as amended, reads as follows, with emphasis added:

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> A method of optimizing instructions included in a program being executed, the method comprising:
> collecting information describing a frequency of occurrence of a plurality of cache misses caused by at least one instruction;
> identifying a performance degrading instruction;
> optimizing the program **during runtime** to provide an optimized sequence of instructions, the optimized sequence of instructions comprising at least one prefetch instruction; and
> modifying the program **being executed** to include the optimized sequence.

Applicants' independent Claim 26 reads as follows, with emphasis added:

> A computer-readable medium having a computer program accessible therefrom, wherein the computer program comprises instructions for:
> collecting information describing a frequency of occurrence of a plurality of cache misses caused by at least one instruction;
> identifying a performance degrading instruction;
> optimizing the computer program to provide an optimized sequence of instructions, the optimized sequence of instructions comprising at least one prefetch instruction; and
> modifying the computer program being executed to include the optimized sequence **during runtime**.

Applicants' independent Claim 27 reads as follows, with emphasis added:

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A computer system comprising:
a processor;
a memory coupled to the processor;
a program comprising instructions, the program being stored in memory, the processor executing instructions to:
collect information describing a frequency of occurrence of a plurality of cache misses caused by at least one instruction;
identify a performance degrading instruction;
optimize the program to provide an optimized sequence of instructions, the optimized sequence of instructions comprising at least one prefetch instruction; and
modify the program being executed to include the optimized sequence **during runtime**.

Applicants respectfully submit that since the limitations of the present amendments to Claims 1, 26 and 27 were not only implicit in these claims when read in light of the disclosure, but were also explicit limitations of Claims 13 and 25, **as filed**, these amendments do not require a new search or raise new issues.

In light of the discussion above, Applicants respectfully submit that the Examiner has failed to show that the prior art reference (Hobbs) teaches or suggests all the claim limitations as discussed above including **dynamic** optimization. Consequently, Applicants respectfully request the Examiner withdraw the rejection of Claims 1, 13, 25, 26, and 27, as amended based on Hobbs and 35 U.S.C. 103(a) and allow Claims 1, 13, 25, 26, and 27 to issue.

In addition, Claims 2 to 12 depend, directly or indirectly, on Claim 1 and Claims 14 to 24 depend, directly or indirectly, on Claim 13. Therefore Applicants respectfully request the Examiner withdraw the rejection of Claims 2 to 12 and 14 to 24 as well.

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CONCLUSION

For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 28, 2005.

Attorney for Applicant(s) — November 28, 2005 Date of Signature

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